FULL-TIME RESEARCH AND TEACHING ASSISTANT POSITION

IN EMBEDDED ELECTRONICS

BRUSSELS SCHOOL OF ENGINEERING

Reference: 2022/S126
Application deadline: 30/08/2022
Start date: 01/10/2022

Job Description

The candidate will be expected to conduct high-quality research, leading to a Ph.D. degree, in the field of Micro-processor architectures for Logic-on-Logic 3D system integration: Current 3D technologies such as Through-Silicon Vias, Front-side and Back-side bumps enable integration of multiple dies in a single package with very dense die-to-die interconnect allowing system partitioning at very fine grain. Such technologies are already used in some commercial products today but focus for now on Memory-on-Logic (MoL) only. Recent example of stacking V-Cache in AMD processors or Intel Foveros technology perfectly illustrate the above approach. The natural extension of MoL would be Logic-on-Logic (LoL) 3D system integration, in which complete Logic and Memory sub-systems could be partitioned to allow integration of true 3D micro-processors. While Logic-on-Logic partitioning of micro-processors has been explored to some extent (e.g. OpenSPARCT T2 core, S.K. Lim et al.) no work has been done on micro-processor architecture modifications for LoL 3D integration.

In this PhD thesis the candidate will have to identify the most important bottlenecks in scaling core architectures in 2D using Berkley-Out-Of-Order Machine (BOOM) configurable core generation framework to propose original core architecture modifications enabled by 3D LoL technology. On the other hand, the candidate will work on enablement of 3D placeable objects (front-side bumps namely) into the OpenRoad open-source EDA place&route flow driven by Prof. A.Khang from UCSD. This flow be then used to provide in-depth, performance, power, and area characterization of the proposed architectures in 3D and compare them with the 2D base-line designs.

The candidate will also take part in educational activities (architectural studios, tutorials, projects, master’s thesis and pedagogical coordination) in the Bachelor and Master’s programme in architectural engineering of the Brussels School of Engineering

Skills required

- Micro-processor architecture and programming in C/C++
- Digital system design using HDLs (VHDL and/or Verilog)
- Digital system implementation flows (FPGAs and/or ASICs)
- Linux OS and scripting using different languages is a plus
- Good scientific writing skills
- Autonomy, reliability, high motivation
- Ability to work in multidisciplinary teams
- C1 level in French and B2 level in English are required, C1 level in English will be appreciated
- Innovative and creative thinking is a must

**Courses covered**

The candidate will participate in the teaching of some of the following courses, to be determined with the supervisor as a function of specialties and interests:

- ELEC-H-201: Electricité
- ELEC-H-2001: Electricité et électronique
- ELEC-H-301: Electronique appliquée
- ELEC-H-305: Circuits logiques et numériques
- ELEC-H-309: Projet intégré
- ELEC-H-310: Digital Electronics
- ELEC-H-314: Instrumentation et électronique analogique
- ELEC-H-402: Analog Electronics
- ELEC-H-409: Digital architectures and design
- ELEC-H-410: Real-time computer systems
- ELEC-H-473: Microprocessor architectures
- ELEC-H-505: Advanced digital architectures
- ELEC-H-516: Programmable Logic Controllers

**Interested?**

For more information, please contact Mr François QUITIN (fquitin@ulb.be) and Mr Dragomir MILOJEVIC (Dragomir.milojevic@ulb.be).

Applications must be sent by e-mail to the rectorate of the Université Libre de Bruxelles (rectrice@ulb.be) and to the faculty deanship (le-doyen-polytech@ulb.be).

They must include the following:

- a motivation letter
- a note on the applicant’s PhD research project (4 pages)
- two letters of reference

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for the academic and scientific staff (marie.botty@ulb.be). Be assured of the confidentiality of this information.


You will find all the regulations relating to research careers on our site at http://www.ulb.ac.be/emploi/academique.html.